VIRTUALOGIC
ASIC EMULATION

VirtuaLogic delivers the capacity needed for complex system-on-chip designs with a powerful, reliable and effective in-circuit emulation solution.

POWERFUL IC PROTOTYPING AND VERIFICATION TOOL FOR MANAGING THE COMPLEXITY OF SUB-MICRON CHIP DESIGNS

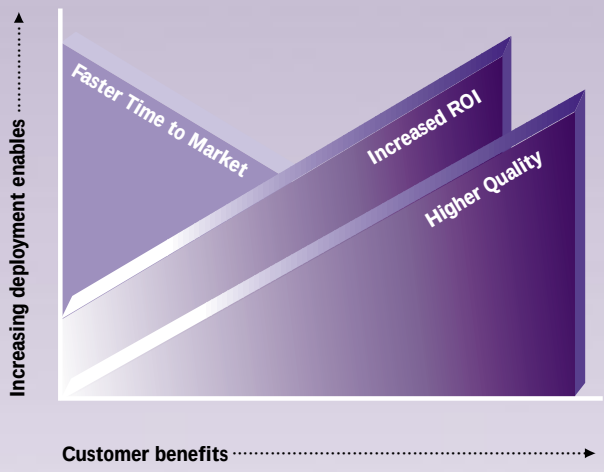
When simulation is not enough, and real world operation is required to verify the designs of highly complex chips, emulation is the only solution. The VirtuaLogic emulator (VLE) provides the performance, capacity and flexibility needed to achieve design confidence while facing intense time-to-market pressures.

Combined with IKOS' patented VirtuaLogic software, VLE provides a complete emulation solution featuring easy memory modeling, effective models of asynchronous clocks, automatic partitioning, fast compilation of emulation models, and powerful analysis of 100% of all internal and external signals. Innovative IKOS emulation technologies ensure predictable operation and reduce emulation time, and user-friendly displays simplify the process – a range of powerful VirtuaLogic features that help your design reach the market faster.

FULLY AUTOMATIC, RELIABLE COMPILATION

The VirtuaLogic compiler is entirely automatic and highly predictable, unlike traditional emulation systems requiring significant user intervention and pathfinding through several software programs. VirtuaLogic's stability is due to the innovative interconnect resynthesis techniques of the patented VirtualWires technology, developed at MIT and available exclusively from IKOS. VirtuaLogic provides a highly reliable compile by isolating the timing variables of the FPGA from the user's design. Each pin is time

- Fastest Time-to-Emulation
- Reliable and Fast Automatic Compilation
- Simple and Powerful Memory Modeling
- User-Friendly GUI
- Up to 5 Million Gate Capacity
- Up to 48 MBytes In-System Memory
- Simulator-Like Debug Environment
- 100% Visibility of All Internal Nodes



"IKOS' VIRTUALOGIC HAS MANY KEY FEATURES THAT MAKE IT A WINNING SOLUTION FOR XYLAN. IT IS THE ONLY EMULATOR THAT PROVIDES ENOUGH MEMORY CAPACITY TO HANDLE OUR COMPLEX DESIGN, AND IT CAN ALSO HANDLE A HUGE NUMBER OF PROBES. WE SELECTED VLE AS OUR EMULATOR PLATFORM OF CHOICE FOR THE VERIFICATION OF OUR NEXT-GENERATION SWITCH/ROUTER PRODUCTS."

Chris Hoogenboom
Director of ASIC Engineering, Xylan

VIRTUALOGIC

multiplexed, further strengthening the predictability of the system and ensuring that once the design is successfully compiled, it will always compile properly.

HIGH COMPILE SPEEDS

VirtuaLogic can compile designs at a speed of one million ASIC gates per hour, while overlapping the place and route of the FPGAs. VirtualWires enables VLE to use significantly less FPGAs than other emulators, and with the use of PCs and workstations for place and route, VirtuaLogic provides highly competitive total compile times. IKOS customers have achieved a total time for compile plus place and route of less than two hours for one million gate designs.

SIMPLE EFFECTIVE MEMORY MODELING

The VirtuaLogic compiler provides a very simple method of modeling internal memories in the design. Any number of read/write ports can be specified with virtually any bit width and word depth. There is no limit to the number of internal memories, or the number of instances used. The VirtuaLogic compiler uses standard SRAMs that are direct-connected to the FPGA.

HIGH-CAPACITY HARDWARE

IKOS offers two hardware platforms to meet the growing capacity requirements of the market. VLE-5M delivers a 4.5-million-gate capacity, and VLE-2M is also available for designs up to 2 million gates. Both platforms offer the same features, differing only in logic and memory capacity.

POWERFUL DEBUG AND ANALYSIS

When the emulated design is plugged into the target system, VirtuaLogic's simulator-like analyzer facilitates quick identification of design bugs. The VirtuaLogic analyzer's 100% visibility and simulator-like display capabilities maximize debug and analysis productivity, allowing designers to quickly isolate problems hidden in complex designs.

Extensive Visibility: VirtuaLogic provides 100% visibility through a software technique called node reconstruction (patent pending) – virtually every signal in the design can be viewed without recompiling or even physically probing the signal.

Simulator-Like Display: The VirtuaLogic analyzer has four windows to view signals and the original design netlist. The Source window provides a textual display of the design, while the Hierarchy window graphically displays the design and all relationships between design array boards. Both the Waveform and Logic Browser windows display captured Virtual-Probes and reconstructed signals.

AVATAR EXPANDS EMULATION POWER

VirtuaLogic's Avatar replicates provide the critical competitive edge of hardware/software co-verification. Avatar delivers Virtual First Silicon to the entire design team, enabling them to begin system and software debug as soon as the chip design becomes stable, rather than having to wait for silicon. The low-cost Avatar solution provides easy implementation of multiple emulation setups. Software debug and regression testing stations can use the same compiled database as the primary VLE installation. Avatar provides all the capability of the VLE system except for the internal probing of nets.

SPECIFICATIONS

		Modularity	ASIC Gate Capacity	Memory Capacity	Emmulation Speed	I/O Connections	Probing	Dimensions	Weight	Power
VLE-5M	Array Board	1	750,000	8 Mbytes		512	5000			
	System	6	4,500,000	48 Mbytes	500 khz - 2 Mhz	3072	30000	10” H x 24.5” D x 22.5” W 25.4cm H x 62.2cm D x 57.2cm W	95 lbs 43.10 kg	90-264 V AC 47-63 Hz 1200 W
VLE-2M	Array Board	1	340,000	2 Mbytes		512	5000			
	System	6	2,040,000	12 Mbytes	500 khz - 2 Mhz	3072	30000			

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